MATLAB design & implementation of flyback dual active bridge converter using ultra capacitor bank for AIRBUS 787 & AIRBUS 383 applications

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The development of All Electric Aircraft has provided new opportunities in the area of electronic devices and power electronics. The purpose of this paper is to compare the properties of soft-switching converter topologies when used to achieve dc-dc conversion at high-power and high-voltage levels. The circuit investigated in this paper can operate in a soft-switching manner enabling reduction in device switching losses and therewith an increase in switching frequency. ZVS soft-switching region of a DAB converter with arbitrary operating waveforms. The effect of the junction capacitor of the device and the magnetizing Inductance of the transformer is also analyzed. Through the analysis, a group of waveforms for different loading conditions are identified to maximize the ZVS operating region. The results are verified by simulation using real device models.

PACS numbers:

I. INTRODUCTION

The power generation capacity electric boing 787 air bass A380 airplanes is above 1.4 MW and 850KW respectively. In order to reduce the weight of the aircraft electric power should be delivered at a high voltage With low current and low conduction losses this technology leads to simpler Equipment and enables significant energy saving device. But request high power density DC/DC converter. For a variety of application such as battery base uninterrupted power.

The dual active bridge (DAB) topology for DC/DC conversion has been popular. Over the past two decades due to high performance, high efficiency galvanic isolation and inherent soft-switching Property. Here trapezoidal and triangular modulation methods to achieve triangular and trapezoidal currents in the DAB convertor AC link. This was achieved by modulating the duty cycle of the converter bridge to reduce losses over a wide operating voltage range. Ultra capacitor constitute one form energy storage device which can be used to make transients to meet power demands and smooth the load on the generators. The analyze is extended to Soft-switching (ZVS) boundaries? by considering the effect of snubber capacitor on the DAV converter.

The minimum current requirement for achieving ZVS under buck and boost modes is also determined. With the increasing need for electric power in future automobiles there is an increasing requirement for bi-directional isolated DC/DC converters to transfer energy between different voltage levels, such as between the low voltage accessories and the high voltage drive train. An alternative application for such type of converters is in future more-electric aircraft where the power converters will be used to interface between the aircraft power distribution bus and specific loads. To reduce the volume of the converter, high switching frequencies are required to decrease the volume of the converter passive components, especially the transformer. The transformer is one of the main power density barriers of the isolated DC/DC converter, and the volume can be reduced by increasing switching frequency up to several hundred kHz. In this work, a prototype DAB converter using Si MOSFETs is under design and construction. In a second stage, Sic MOSFETs will be used to reduce the conduction loss and increase the overall converter power density. The switching frequency will be raised to500kHz For switching frequencies that are as high as 500 kHz, the switching loss represents a significant part of the total converter losses, and the volume advantage of the smaller transformer could be defeated by the increase in the size of the heat sink. However, the DAB converter can operate in ZVSsoft-switching mode?in all the power switches?reducing the switching loss. The original modulation scheme presented in can only achieve ZVS within a limited region, as it recurs to hard switching while operating under very light load conditions. Many efforts have been made to extend the soft-switching region, but the full load range remains to be covered In view of the above, this paper presents the soft-switching capability analysis of the DAB converter under arbitrary voltage waveforms, proposing a modulation scheme to further extend the ZVS region of this converter. SOFT SWITCHING REGION ANALYSIS To summarize the existing modulation schemes, the voltage on the primary and secondary winding of the transformer can be drawn as a unified waveform as shown below in fig. 1.

The flyback converter is used in both AC/DC and DC/DC conversion with galvanic isolation between the input and any outputs. More precisely, the fly back converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation. When driving for example a plasma lamp or a voltage multiplier the rectifying diode of the buck-boost converter is

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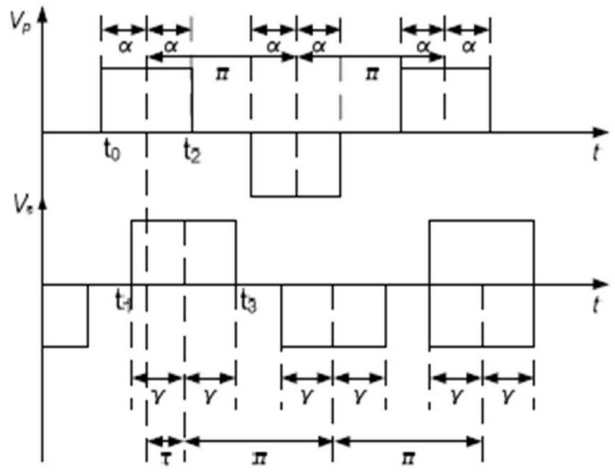


FIG. 1: Unified modulation waveform.

left out and the device is called a flyback transformer.

II. NEW STEADY-STATE MODEL OF FLYBACKDAB CONVERTER

A. Basic Principle of Operation

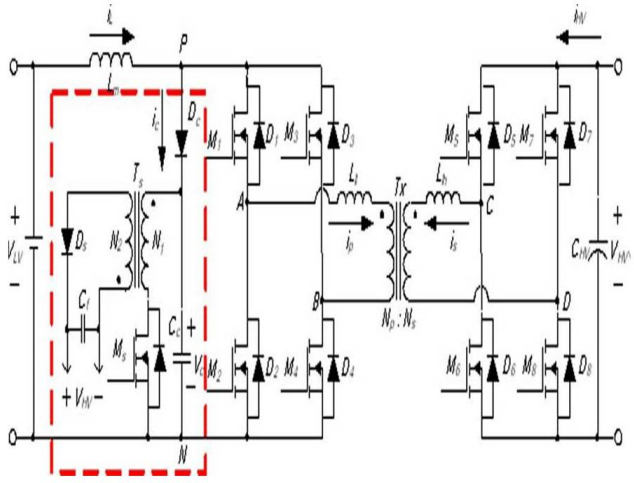


FIG. 2: Circuit diagram for FLYBACK DAB converter.

Future aircraft are likely to employ electrically powered actuators for adjusting flight control surfaces and other high-power transient loads. To meet the peak power demands of aircraft electric loads and to absorb regenerated power, an ultra capacitor based energy storage system is examined in which a bidirectional DAB dc?dc converter is used. The DAB converter shown in Fig. 1 consists of two full-bridge circuits connected through an isolation transformer and a coupling inductor L, which may be

provided partly or entirely by the transformer leakage inductance. The full bridge on the left hand side of Fig. 1 is connected to the HV dc bus and the full bridge on the right hand side is connected to the low-voltage (LV) ultra capacitor. Each bridge is controlled to generate an HF square-wave voltage at its terminals. By incorporating an appropriate value of coupling inductance, the two square-waves can be suitably phase Shifted with respect to each other to control power flow from one dc source to another. Thus, bidirectional power flow is enabled through a small lightweight HF transformer and inductor combination, and power flows from the bridge generating the leading square-wave. Although various modes of operation of the DAB converter have been presented recently for high power operation, the square-wave mode is supposedly the best Operating mode. This is because imposing quasi-square-wave on the transformer primary and secondary voltages results in trapezoidal, triangular, and sinusoidal waveforms of inductor current in the DAB converter ac link. These modes are beneficial for extending the low-power operating range of the converter. Although these modes tend to reduce the switching losses, the voltage loss is significant due to zero voltage periods in the quasi-square-wave, which reduces the effective power transfer at high-power levels. Therefore, the contribution highlighted in this paper forms important research on the DAB converter. The key operating waveforms of the converter during buck mode, i.e., when power flows from the HV side to the LV side are shown in Fig. 2. The voltages generated by the two full bridges, VHV on the HV side and VLV on the LV side, are represented as square-wave voltages with 50% duty cycle. The current flowing through the coupling inductance is i_L,i_{AD1-A1} and i_{CD1-C1} are the device currents on the HV and LV sides, respectively, and i_0 is the output current. The time delay between VHV and VLVis $dT_S/2$, where T_S is the switching period and d is the duty ratio.

B. Steady-State Model

Models for device rms and average currents and peak and rms currents of the coupling inductor are derived based on the assumption of lossless components and a piecewise linear waveform for iL. The difference in voltage between the two bridges appears across the coupling inductor and the inductor current changes with an essentially constant slope; this enables expressions for inductor current peaks corresponding to different switching instants to be determined. When the converter operates in buck mode, the voltage across inductor L over a half cycle is analyzed to determine the peakto-peak change in inductor current. Expressions for inductor current are then derived for switching instants I_P and I_L [1]. The notations used in the following analysis are indicated in Fig. 2. The current at the HV switching instant is expressed as follows:

$$I_P = T_S 4L[nV_{in} + V_0(2d-1)] \quad (1)$$

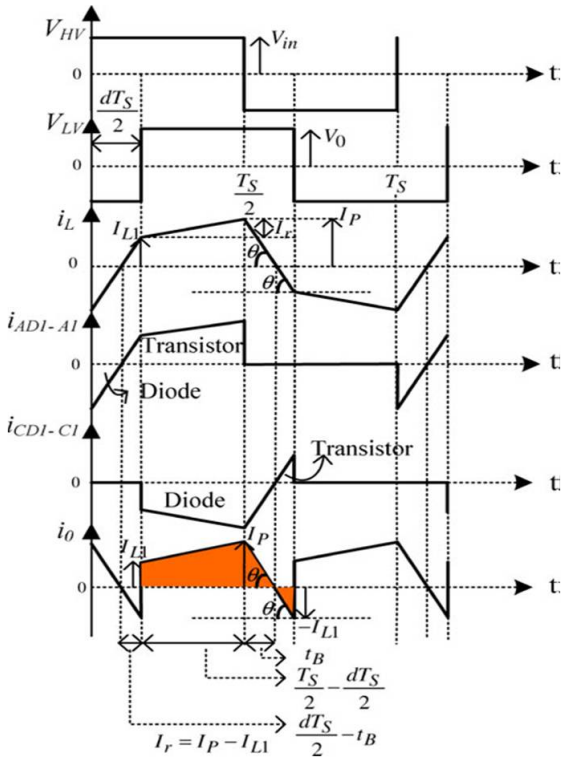


FIG. 3: Key operating waveforms of the FLYBACK DAB converter during buck mode.

wheren is the transformer turns ratio. Solving for the LV switching instant current based on the current slope during the interval $dT_S/2$ gives

$$I_{L1} = T_S 4L[nV_{in}(2d-1) + V_0] \tag{2}$$

In order to find the average output (ultracapacitor) current, the current expression is required for the interval t_B: the time taken for i_L to fall to zero following the HV bridge switching instant. Since the output current waveform is piecewise linear, this can be calculated from the following:

$$I_P + I_{L1}(dT_S/2) = I_P t_B = tan\theta \tag{3}$$

where θ is the angle marked on the i_0 and iLcurrent waveforms shown in Fig. 2. The total current change during the interval $dT_S/2$, where the current is increased from ?I_P to + I_{L1} , can be written as follows:

$$I_P + I_{L1} = nV_{in} + V_0 L_d T_S \tag{4}$$

Substituting (1) and (4) in (3), and solving for t_B gives

$$t_B = T_S[nV_{in} + V_0(2d?1)]4(nV_{in} + V_0) \tag{5}$$

Using the above equations, the area under the i_0 current waveform, shown as a shaded region in Fig. 2, is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $T_S/2$, gives the average output current of the DAB converter,

TABLE I: RMS CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BUCK MODE (POWER TRANSFER FROM THE HV SIDE TO THE LV SIDE).

Device	RMS current equation
HV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)\right]}$
HV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_P^2}{3}\times(t_B)\right]}$
LV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)\right]}$
LV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\frac{(I_P)^2\times t_B}{3}\right]}$

TABLE II: AVERAGE CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BUCK MODE (POWER TRANSFER FROM THE HV SIDE TO THE LV SIDE).

Device	Average current expression
HV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\frac{T_S}{2}-t_B}$
HV side Diode	$I_{avg}=\frac{\frac{1}{2}\times I_P\times t_B}{t_B}$
LV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side Diode	$I_{avg}=\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)+\frac{1}{2}\times I_P\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$

C. ZVS Limits

During transistor turn-OFF, resonance will naturally occur between device output capacitance and coupling inductance. energy stored in the coupling inductance is sufficient to ensure charge/discharge of device output capacitances at the switching instants. The converter

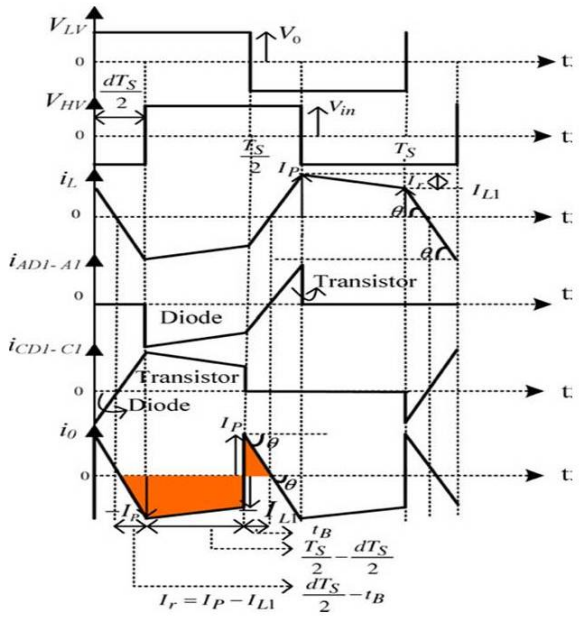


FIG. 4: Operating waveforms of the FLYBACK DAB converter under boost mode.

TABLE III: RMS CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BOOST MODE (POWER TRANSFER FROM THE LV SIDE TO THE HV SIDE).

Device	RMS current equation
HV side Transistor	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_P)^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)\right]}$
HV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P{}^2+\frac{I_r{}^2}{3}-I_P I_r\right)+\frac{(I_{L1})^2\times t_B}{3}\right]}$
LV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_P)^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P{}^2+\frac{I_r{}^2}{3}-I_P I_r\right)\right]}$
LV side Diode	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L1}{}^2}{3}\times(t_B)\right]}$

operating conditions to achieve virtually loss-less ZVS conditions are: 1) atturn-ON of any device, its antiparallel diode is conducting; 2) atturn-OFF of any device, the minimum current flow through the device is positive. In practice, the ZVS limits will be slightly different due to the requirement for inductor current to be sufficient to ensure charge/discharge of the device output capacitances at the switching instants. By applying the ZVS conditions to the device current waveforms, shown in Fig. 2, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV-side bridge.

TABLE IV: AVERAGE CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BOOST MODE (POWER TRANSFER FROM THE LV SIDE TO THE HV SIDE).

Device	Average current expression
HV side Transistor	$I_{avg} = \frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
HV side Diode	$I_{avg} = \frac{\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)+\frac{1}{2}\times I_{L1}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
LV side Transistor	$I_{avg} = \frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\left(\frac{T_S}{2}-t_B\right)}$
LV side Diode	$I_{avg} = \frac{\frac{1}{2}\times I_{L1}\times t_B}{t_B}$

Therefore, based on (2), the following condition must be satisfied for achieving ZVS in the LV side:

$$I_{L1} = T_S 4L[nV_{in}(2d-1)+V_0] \geq 0 \tag{6}$$

Solving for the inequality given in (20), the duty ratio at which ZVS occurs is obtained as follows:

$$d \geq 0.5?V_0 2$$

where $V_0 = V_0/nV_{in}$ is the normalized voltage conversion ratio.

To achieve ZVS in the HV bridge, the current at the HV switching instant given in (1) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given by (21).

For power transfer from the HV side to the LV side, (21) is applicable when $V0 \leq 1$. If $V0 \geq 1$, the shape of the inductor current in Fig. 2 will change, as shown in Fig. 3, and the effect of this is to interchange the expressions for the currents at the LV and HV switching instants. Therefore, with $V_0 \geq 1$, the expression for the LV switching instant current is given by (1) and the expression for the HV switching instant current is given by (2). The ZVS limit still occurs in the LV bridge, but is now specified by requiring the current level in (1) to be greater than zero, When the power transfers from the LV side to the HV side, the ZVS limit is again found to occur in the LV bridge and may be expressed by (20)?(22). Although turn-ON of transistors in the DAB converter is achieved at minimum (near-zero) positive diode current, the instantaneous transistor currents that occur during the turn-OFF process are significant. Normally, the device output capacitance is too low to produce a low dv/dt. Hence, minimal transistor currents during the turn-OFF switching time instant are

mandatory in order to achieve low switching losses. To limit switching transients, reduce current/voltage spikes, and to minimize electromagnetic compatibility (EMC) problems associated with high dv/dt, snubber capacitors can be placed across the switching devices. These capacitors slow down the rate of voltage rise across the devices so that a lower voltage appears during the current decay time. Although snubber capacitors suppress voltage transients during switching, inclusion of a snubber across the switching transistors requires more energy to be stored in the coupling inductance to achieve soft switching [3]. The analysis was performed by assuming that the input (HV) and output (LV) voltages are constant during the transistor turn- OFF instants to estimate the minimum current necessary during turn-OFF to achieve ZVS. To achieve ZVS, energy stored in the inductor must equal the energy delivered to charge and discharge the snubber and device output capacitances.

Where L is the primary referred coupling inductance and v_0 is the primary referred LV bridge voltage source. It has beenassumed in the analysis that the insulated gate bipolar transistor(IGBT) tail current does not change when the snubber capacitoris added. The snubber creates oscillations due to the resonance induced between parasitic inductance of the IGBT module and the snubber capacitance during turn-OFF transient. In practice, the IGBT tail current may be reduced with the addition of an appropriate value of snubber capacitor. However, the tail time increases due to reduced dv/dt. Therefore, to simplify the analysis, the assumption that the IGBT tail current does not change with the inclusion of the snubber capacitor is made. The inductor current should be greater than or equal to the value of IL in (23) during transistor turn-OFF to achieve ZVS. This paper extends the analysis further to obtain the equations of duty ratio for HV and LV device ZVS limits for a specified value of snubber capacitor. Without the snubber, the condition to be satisfied for achieving ZVS during buck mode is given by (20). From (20) and (23), the ZVS boundary condition for $V_0 \leq 1$ while considering the inclusion of snubber is given by

$$I_{L1} = T_S 4L[V_0 + nV_{in}(2d-1)] \geq 2v_0 V_{in} L/C_S. \quad (7)$$

III. SIMULATION RESULTS

IV. EXPERIMENTAL VALIDATION

A. DAB Converter Prototype Design A DAB converter prototype was designed and constructed based on the proposed model to transfer 20 kW of power with a switching frequency of 20 kHz for an input (HV) voltage of 540V and a nominal output (LV) voltage of 125V. These figures are typical of likely future aerospace systems at the HV side and the capabilities of ultracapacitor modules at the LVside. The converter is designed to meet the peak power demandsof aircraft electric loads such as actuators and is based on data from the Intelligent Electrical PowerNetworks Evaluation Facility of Rolls-Royce University Technology Centre, University of Manchester. Assuming a 2:1 working range for the ultra capacitorvoltage, the worst-case operating condition of the converter is: VHV = 540V, VLV = 62.5V, I_{rms} = 427 A, I0 = 320 A, P0 = 20kW, and IP = 640 A, where d = 0.5. The

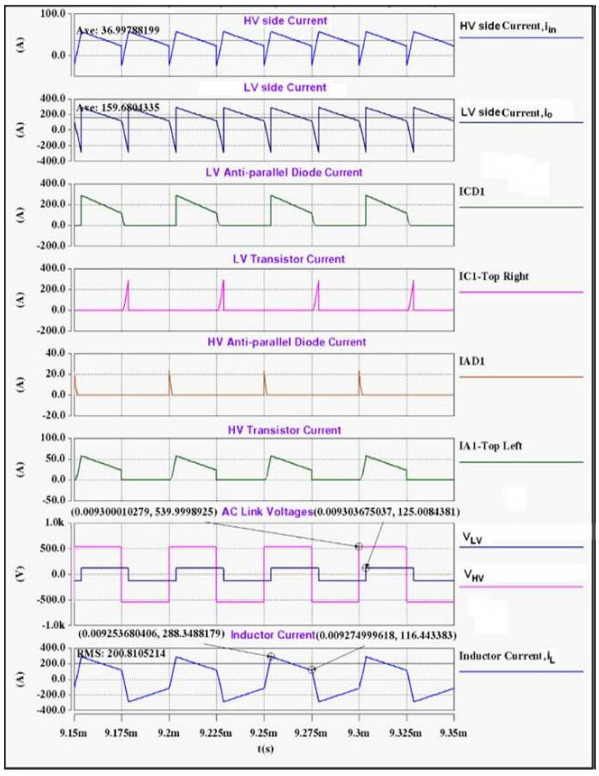
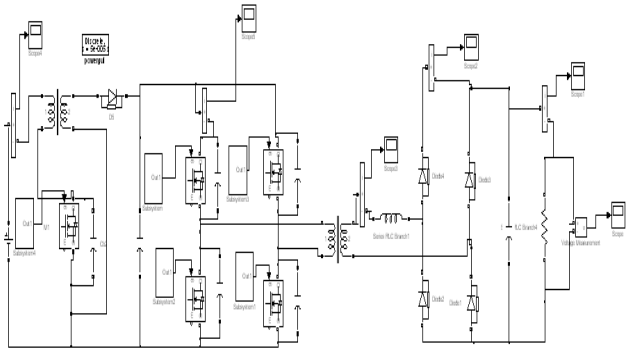
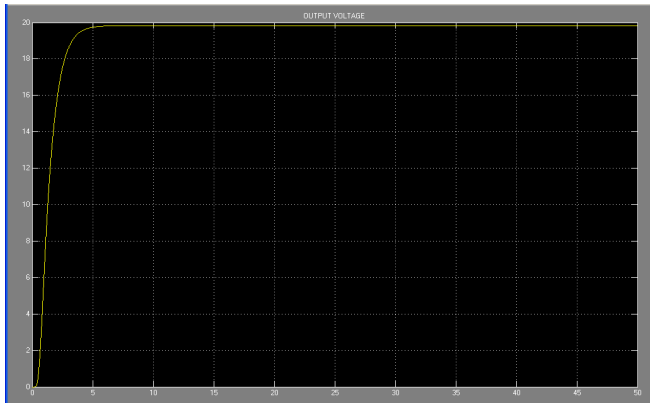


FIG. 5: Simulation results of the converter under buck mode. V_{HV} = 540V, n = 1: 0.2, V_{LV} = 125V, d = 0.146, P_0 = 20kW, I_0 = 160 A, f_s= 20 kHz,and L = 2.11 μH.

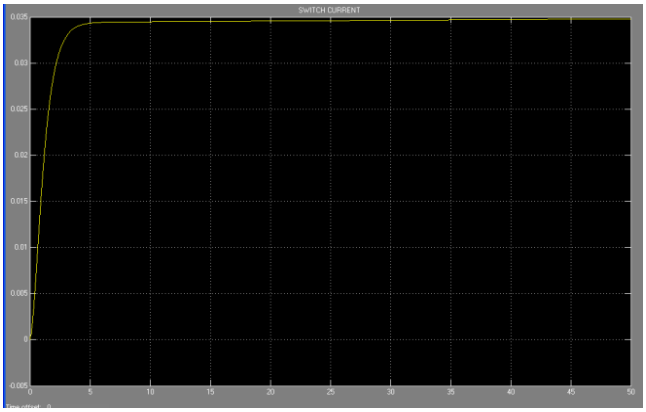
FORWARD DIRECTION FLY BACK (BUCK OPERATION)



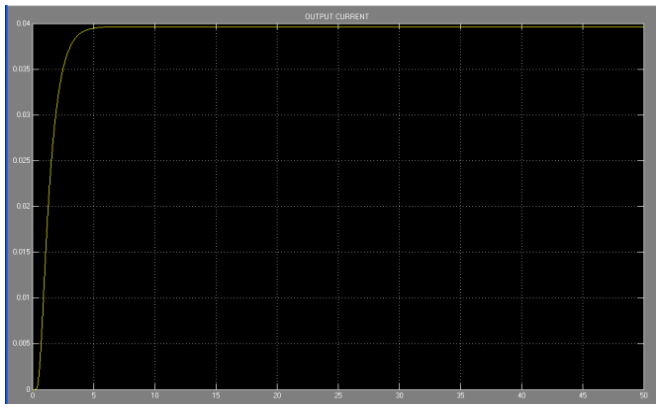
OUTPUT VOLTAGE OF FORWARD DIRECTION



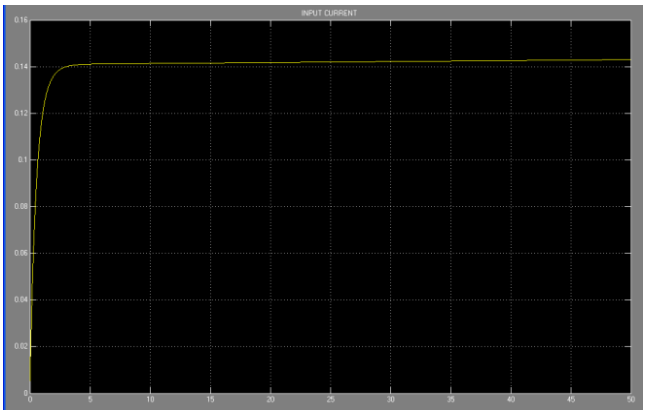
SWITCH CURRENT OF FORWARD DIRECTION



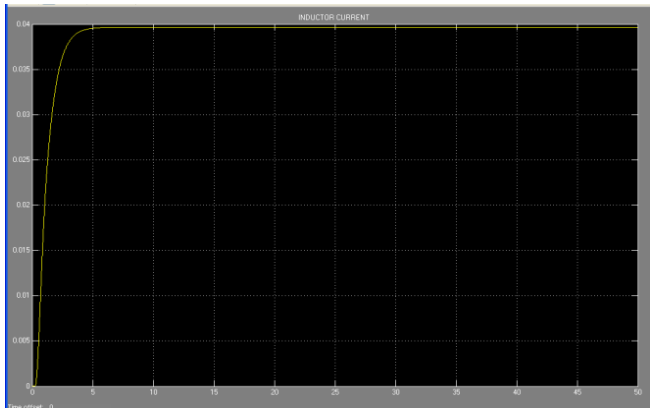
OUTPUT CURRENT OF FORWARD DIRECTION



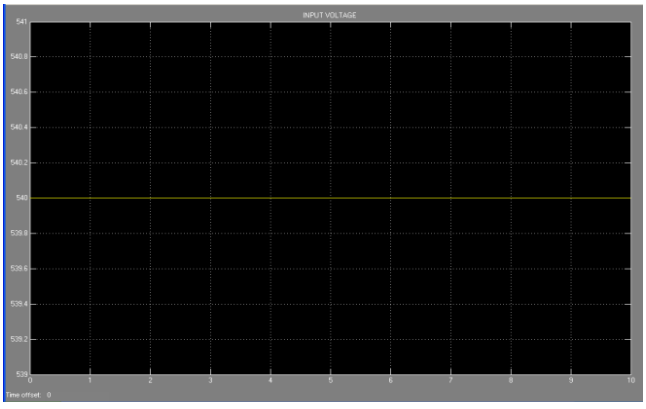
INPUT CURRENT OF FORWARD DIRECTION



INDUCTOR CURRENT OF FORWARD DIRECTION

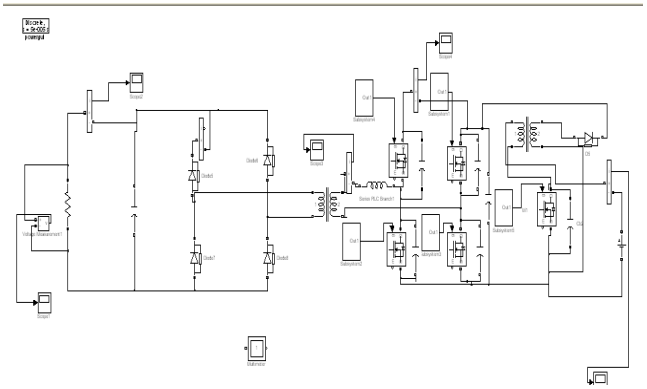


INPUT VOLTAGE OF FORWARD DIRECTION

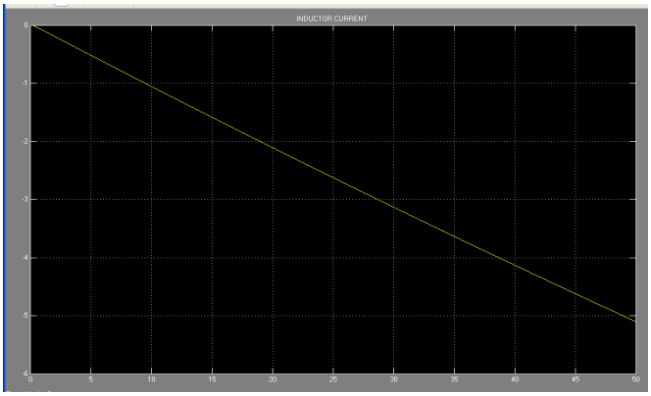


converter design is based on the new model presented in Section II. Key component values of the converter are determined by applying the worst case operating condition to the equations derived from the steady-state model.

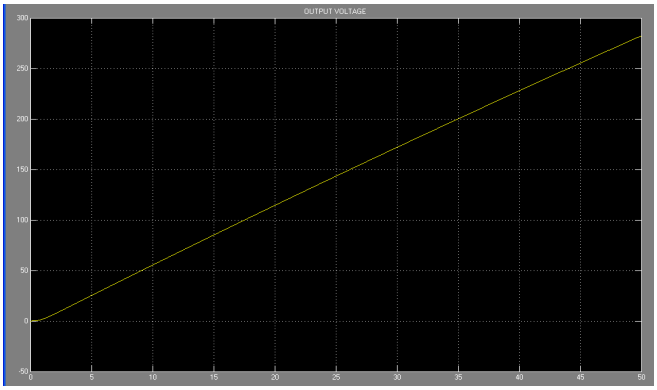
REVERSE DIRECTION(BOOST OPERATION)



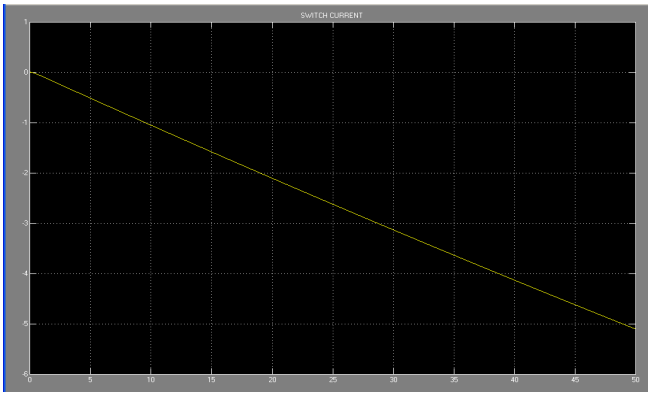
INDUCTOR CURRENT OF REVERSE DIRECTION



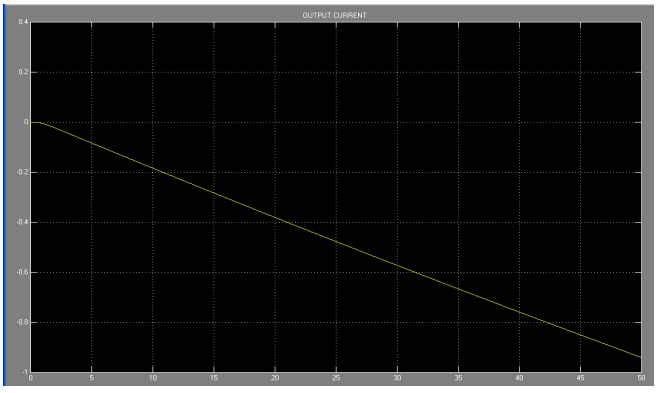
OUTPUT VOLTAGE OF REVERSE DIRECTION



SWITCH CURRENT OF REVERSE DIRECTION



OUTPUT CURRENT OF REVERSE DIRECTION



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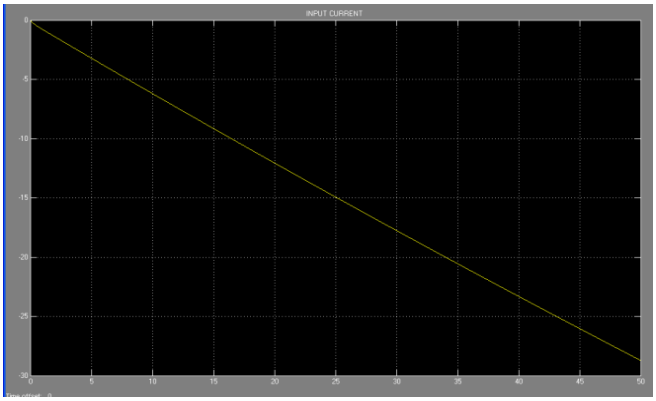
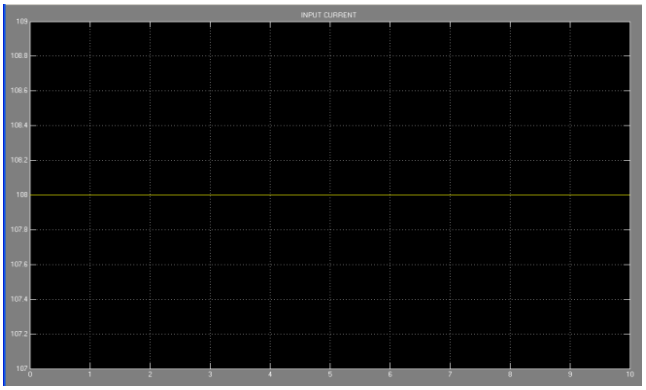


From (6), the coupling inductance is calculated as 2.11 μH for the worst case scenario of maximum power and minimum ultra capacitor voltage. At this operating condition, d was assumed to be 0.5. Using the average and

INPUT VOLTAGE OF REVERSE DIRECTION



rms current values on the HV and LV sides, the rms currents flowing through the HV- and LV-side filter capacitors were estimated as 77 and 283 A, respectively. For the worst case, to maintain 1% ripple voltage, capacitors of 123 μF and 2.91 mF, are required for the HV and LV sides, respectively. Low ESR filters were used on both the HV- and LV-side bridges. Based on the model, the conduction loss of devices can be calculated using the average current equations given in Tables II and IV. The switching loss calculation was made using the energy loss curves from the device datasheet for the operating frequency of 20 kHz. Ultrafast 1200V, 300A phase leg IGBT modules (SKM300GB125D) from Semikron have been selected for the HV-side bridge and fourth generation high temperature 600V, 760A phase leg IGBT modules (SKM600GB066D) from Semikron have been chosen for the LV-side bridge. Simple lossless snubber capacitors were selected to reduce the turn-OFF switching loss of the IGBTs. The peak current flowing through snubbers at the time of turn-OFF, determined from the model, and the corresponding dv/dtwere estimated for the worst-case operating condition. 47 nF and 100 nF-polypropylene pulse capacitors have been chosen for the HV and LV sides, respectively. Considering the snubber capacitor charging time, a dead time of 2.2 μs between the top and bottom IGBTs of a phase

leg was chosen. The switching time of the LV-side IGBT as per the manufacturer?s datasheet is about 1 ?s. The dead time needs to be longer than the transistor switching time. Although inclusion of snubber capacitor across the IGBT reduces the initial current fall time, it significantly increases the tail current suppression time due to reduced dv/dt. In addition, the dead time generated by RC networks of the IGBT driver was incorporated into the design. To minimize circuit parasitics, the circuit connections were configured using planar busbars. The entire converter is forced air-cooled. The devices on the HV and LV sides of the DAB converter were individually tested with an inductive load to their full voltages and maximum currents, and the corresponding results were presented in

V. EXPERIMENTAL RESULTS

To practically validate the new steady-state model presented in Section II, experimental results were obtained for a power transfer of 7kW at 20 kHz for d = 0.5, VHV = 390V, and VLV = 180.77V with a resistive load of R = 5 ? connected on the LV-side bridge. Experimental testing of the converter was performed with the two active bridges interfaced through a transformer of 1:1 turns ratio with an air core coupling inductor L = 61.2 μH. A dc blocking capacitor was connected in series with transformer windings to prevent transformer saturation. A common-mode choke was connected to both supply rails and a damping filter was introduced to improve the EMC of the converter. The experimental results are presented mainly to demonstrate the effectiveness of the steady-state model, and therefore results for the DAB converter operating under buck mode alone are presented in this section as results for operation under boost mode can be obtained in a similar manner. Fig. 7 shows a photograph of the prototype and Table VI highlights its main features. Table VII gives the parameters for experimental testing of the DAB converter.

VI. CONCLUSION

This project presented a steady state analysis for the DAB converter. The expressions for the average and RMS device currents along with the peak and RMS currents of the coupling inductor were obtained through analysis. Experimental results are presented for working conditions of the prototype with a measured efficiency of 90%. Simulation and experimental results exhibit a fine correlation, which demonstrate the proposed analysis equations are useful.in predicting losses that occur in the devices and passive components and enable a study of the converter characteristics, in addition to aiding in the practical design of converter prototypes. The influence of the snubber capacitor was analyzed in detail and the minimum current required to operate the converter in the soft-switching region, and its corresponding duty ratio for buck and boost modes, has been determined. The operation of theDAB dc?dc converter has been verified through extensive simulations which, in turn, confirm the accuracy of the model. The experimental results confirm that provision of snubber capacitors across the IGBTs reduces switching losses and device stresses and improves the converter performance.

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